

Caavo Labs India

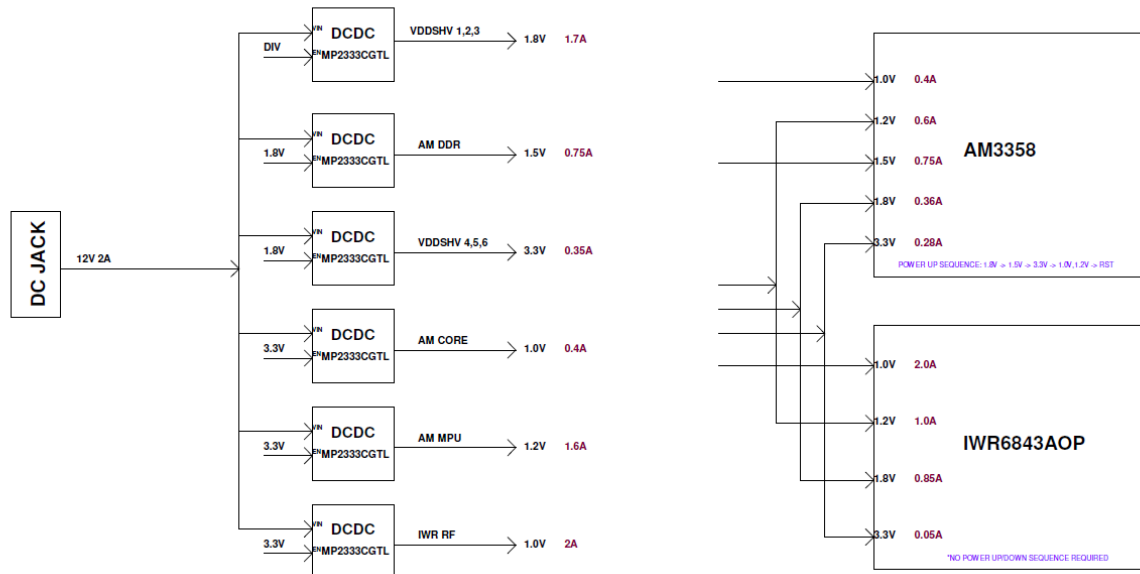
Document: Vendor Schematic Review

Design name: CAVECSSH00E00

Revision History

Revision No	Description	Date
0.1	Initial Design	09/09/21

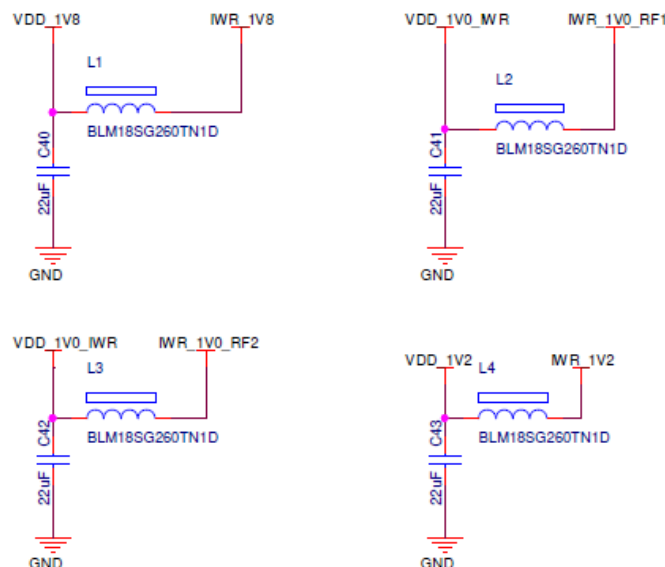
Q1. In our design we are not providing power up sequence for AM3358 assuming that power on reset is enabled only after all voltages are stable. Are there any consequences ?



Page no: 3 Power tree

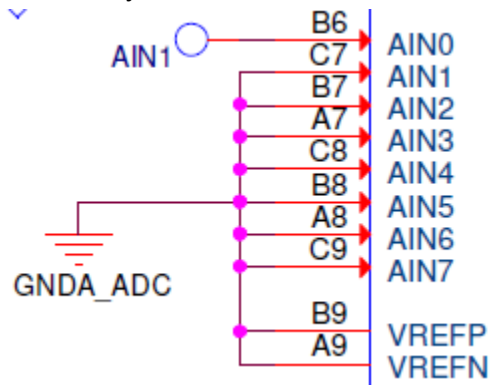
Q2. We are using a DCDC regulator instead of the PMIC. We are using a bead (BLM15PD300SZ1D) on 1.2V and 1.8V. Do we have to provide an LDO bypass circuit for 1.2V and 1.8V?

LDO BYPASS



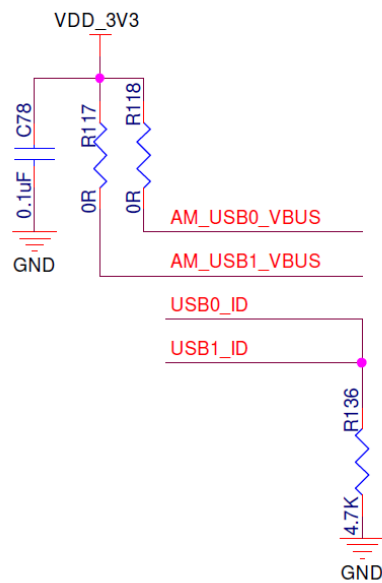
Page no: 5 IWR POWER

Q3. We are not using ADC functionality so we have connected ADC VREFP/N to GND, is it OK?



Page no: 7 AM IO

Q4. We are not using USB functionality so we have connected USB ID to GND and USB VBUS to 3.3V, is it OK?



Page no: 7 AM IO

Q5. We have not connected the VSS_OSC pin to board GND. As per the datasheet we have to connect VSS_OSC to GND. But in EVM Schematic, VSS_OSC is not connected with Board GND. Do we need to connect the VSS_OSC pin to GND?

